IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Myles Kimmitt

Serial No.: 10/620,635 Group No.: 2616

Filed: July 16, 2003 Examiner: Su, Benjamin

For: PHYSICAL CODING SUB-LAYER FOR TRANSMISSION OF DATA OVER MULTI-CHANNEL MEDIA

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Pre-Appeal Brief Request for Review

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Commissioner for Patents
PO Box 1450
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Dear Sir:

The Applicants hereby submit the reasons for our concurrently filed Pre-Appeal Request for Review to the United States Patent and Trademark Office. This Pre-Appeal Brief is in response to the Final Office Action mailed April 7, 2009. Concurrent with the filing of this Pre-Appeal Brief is a Notice of Appeal (Form SB/31), a Pre-Appeal Brief Request for Review (Form SB/33) and a petition for an Extension of Time for THREE (3) Months.

1. Status of the Claims

Claims 1 and 2 are pending. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchanan, et al., (U.S. 6,970,435 – "Buchanan") in view of Partyka (U.S. 5,659,580). Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchanan, et al., (U.S. 6,970,435 – "Buchanan") in view of Partyka (U.S. 5,659,580) and further in view of Nishida, et al., (U.S. 5,978,486 – "Nishida").

2. The Examiner's assertion of Buchanan teaching is a clear error of fact

Regarding claim 1 and 2, the invention generates lesser width parallel data words from a greater width parallel data word by interleaving bits of the greater width parallel data word across the lesser width parallel data words ***such that each successive bit*** of said greater width parallel data word ***is contained within a different one of*** said lesser width parallel data words. Buchanan describes partitioning a 16 bit data stream into four groups of four bit nibbles, see col. 4, lines 50-66, below:

> interface is on a byte (8-bit) boundary. According to the present invention, it is more advantageous to partition the bits into nibbles for processing and sending through the serial link. In one embodiment of the present invention, 16-bit parallel data streams are supplied to DASI. interface. The bit streams are partitioned into four groups of four bit (4 bits-1 nibble) streams. Each of the nibbles is processed according to the teaching of the present invention and is sent over a serial link. As a consequence, to transmit the 16-bit, four serial links would be required. Each nibble of data is processed in the same way; therefore, the description of one (set forth hereinafter) is intended to cover the processing of the others. The four parallel data bit streams are transformed into a high speed serial bit stream by latching each of the four bit streams in one of the Latch L1 through L4 and sequentially strobing the latched information at four time the parallel clock rate using Multiplexer Circuit 22. The data

Therefore, Buchanan teaches partitioning a 16 bit parallel data word into 4 bit nibbles using one of latches L1-L4 for each nibble, and then sequentially strobing the latched nibbles using the multiplexer circuit 22. The four bit nibbles will thus ***include successive*** bits of the 16 bit parallel data word.

In contrast, the invention generates lesser width parallel data words by interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of

said lesser width parallel data words. Then, the lesser width parallel data words are serialized and transmitted. The assertion that Buchanan teaches what is claimed is clear error.

3. Partyka fails to cure the defects of Buchanan

Claimed is interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words. In contrast, Partyka explicitly teaches interleaving ***contiguous buffer addresses*** to change an output transmission order of data bits in a single data block for transmission , see col. 4, lines 2-20, below:

> ated by contiguous counter **214**. In other words, encoded data **142** is stored in contiguous order in data buffer **202**, i.e., bit **0** of encoded data stream **142** is stored in the first bit address location in data buffer **202**, bit **1** of the encoded data stream **142** is stored in the second bit address location, bit **2** of the encoded data stream **142** is stored in the third bit address location, etc.
>
> After encoded data **142** is completely stored in data buffer **202**, multiplexer **210** connects address twister **216** to address bus **208** of data buffer **202**. Address twister **216** is a state machine which generates a noncontiguous sequence of addresses which corresponds to an interleaving sequence. Thus, encoded data **142** is output from data buffer **202** in an order defined by the interleaving sequence generated by address twister **216**. In other words, the interleaving sequence generated by address twister **216** is used to address data buffer **202** as encoded data **142** is output from data buffer **202**. Thus, data is output from data buffer **202** in a sequence that corresponds to the interleaving sequence generated by address twister **216**.

Partyka teaches a method for re-ordering data in a serial transmission.

The Examiner has repeatedly referenced serial transmission schemes to attempt to teach the claimed ***parallel word generation*** according to the invention. A person of ordinary skill in the art would readily understand that the invention generates lesser width parallel words by interleaving bits of a greater width parallel data word according to the claims. Partyka has nothing to with parallel data words, as claimed. Partyka reorders bits of a data block for transmission by interleaving contiguous buffer addresses. Therefore, the rejection of claim 1 should be reconsidered and withdrawn.

4. Nishida Fails to Cure the Defects of Buchanan and Partyka

Regarding claim 2, Nishida is referenced only to teach scrambling the data in the lesser width parallel data words. Nishida teaches a scrambling parallel data, see e.g. col. 18, lines 33-39, below:

A fourth embodiment of the present invention relates to a data scrambling apparatus that receives information data to be scrambled, by 8 bits in parallel and outputs scrambled data by 8 bits in parallel. FIG. 7 shows an example of the data scrambling apparatus. In order to facilitate and embody the explanation, a generating polynomial, $G(X)=1+X^{-4}+X^{-}$ $_{8}$, is employed.

Scrambling data, including parallel data, is known. What Nishida, alone or in combination with Buchanan and Partyka, fails to make obvious is scrambling lesser width parallel data words concurrently generated from a greater width parallel data word 'by interleaving bits of the greater width parallel data word across the lesser width parallel data words such that each successive bit of said greater width parallel data word is contained within a different one of said lesser width parallel data words' as claimed. At best, the proposed combination might teach scrambling ***partitioned*** parallel data words, but can never teach or suggest what is claimed. Therefore, the rejection of claim 2 should be reconsidered and withdrawn as the premise that Buchanan teaches interleaving bits of the greater width parallel data word across the lesser width parallel data words ***such that each successive bit*** of said greater width parallel data word ***is contained within a different one of*** said lesser width parallel data words is clear error.

3. Conclusion

The Applicant has demonstrated clear error in the Examiner's reasoning for rejecting Independent claims 1 and 2. It is believed that this application is now in condition for allowance. A notice to this effect is respectfully requested. Should further questions arise concerning this application, the Examiner is invited to call Applicant's attorney at the number listed below. Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 50-3650.

Respectfully submitted,
3Com Corporation,

By

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